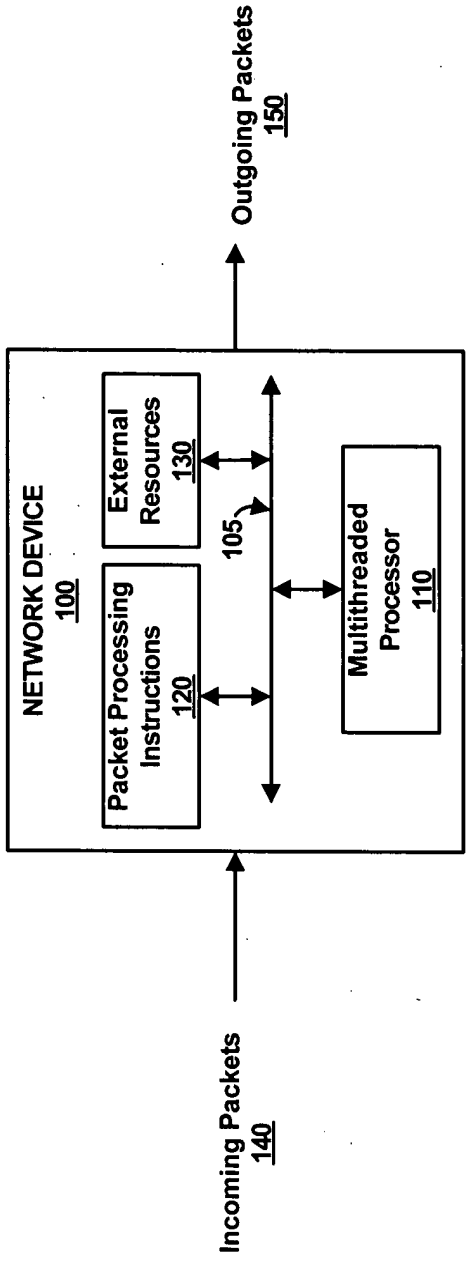
Outgoing Packets
150
NETWORK DEVICE
100
External Resources
130
105
Packet Processing Instructions
120
Multithreaded Processor
110
Incoming Packets
140

FIG. 1

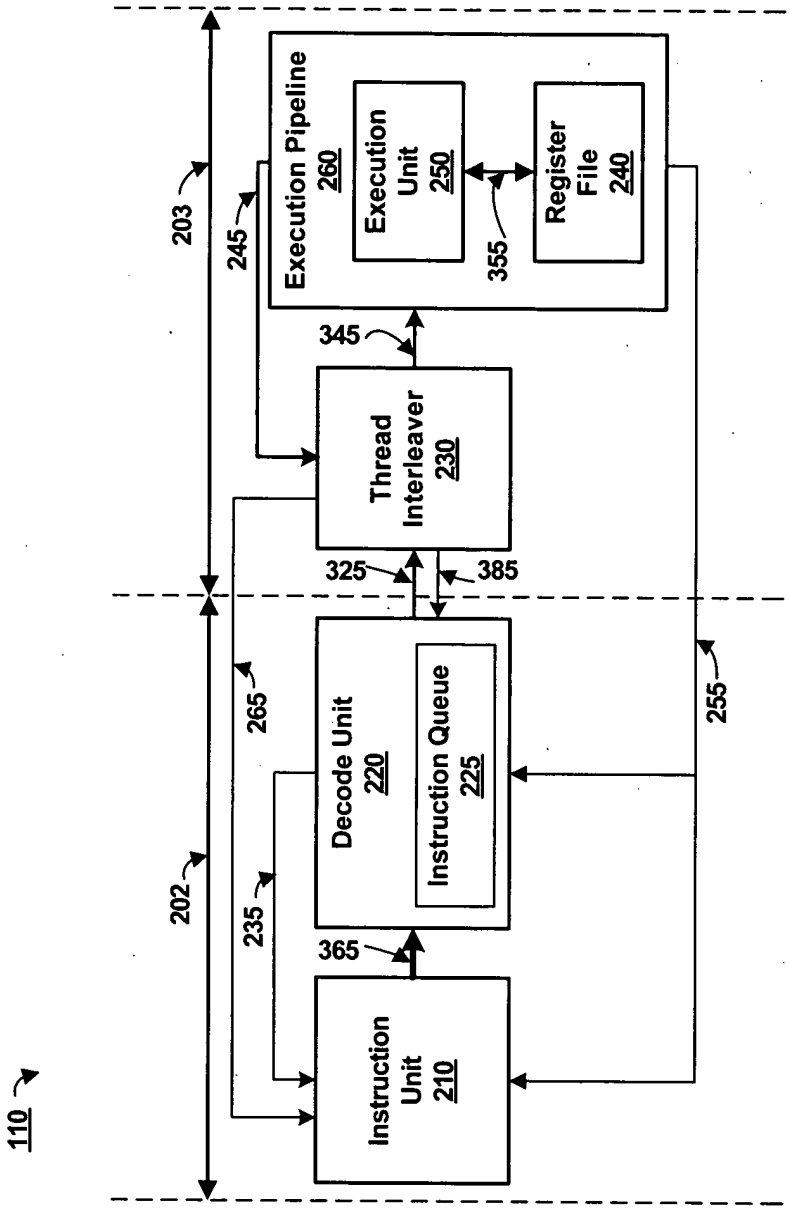
110
Instruction Unit 210
Decode Unit 220
Instruction Queue 225
Thread Interleaver 230
Execution Pipeline 260
Execution Unit 250
Register File 240
202
203
235
245
255
265
325
345
355
365
385

FIG. 2

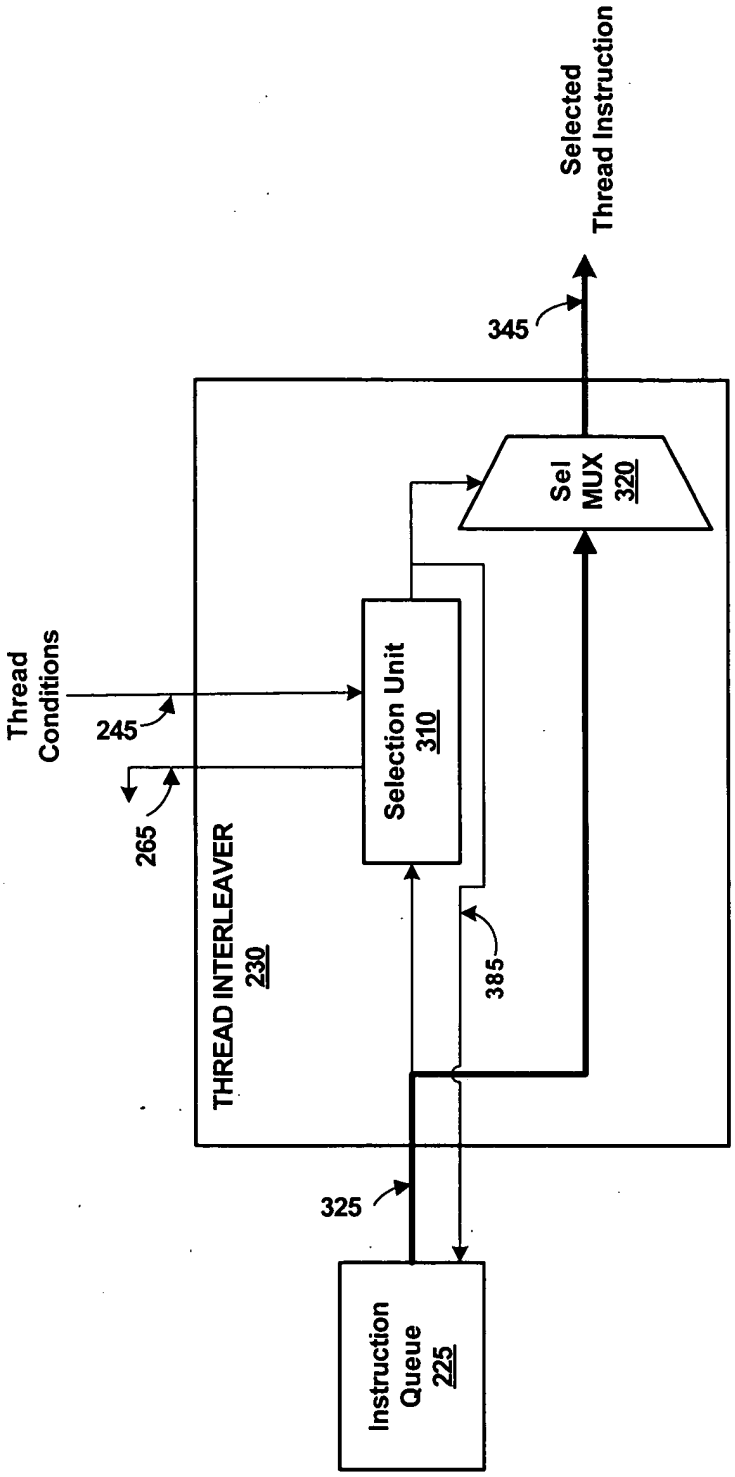
Selected Thread Instruction
345
Sel MUX 320
Thread Conditions
245
265
Selection Unit 310
THREAD INTERLEAVER 230
385
325
Instruction Queue 225

FIG. 3

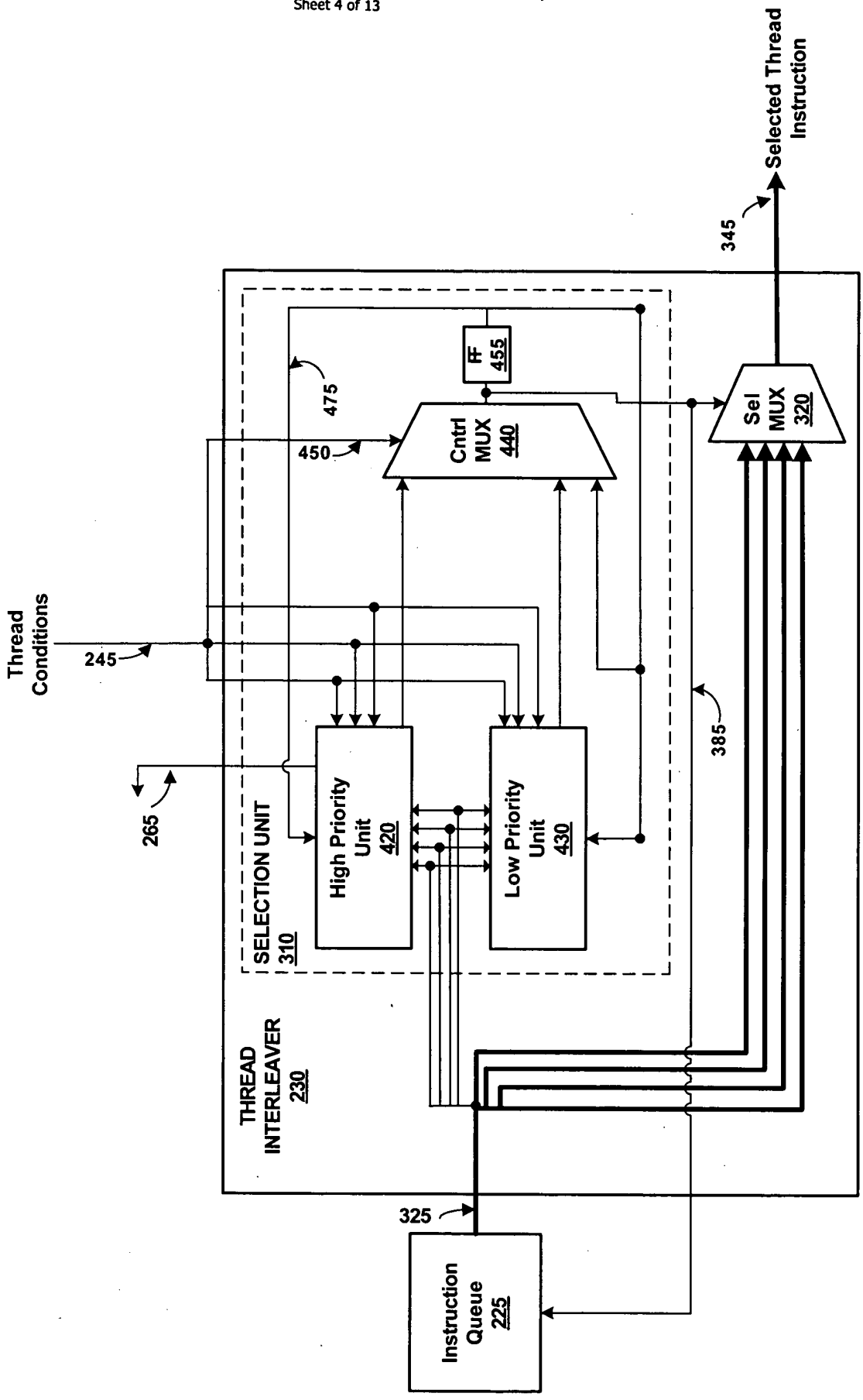
Selected Thread Instruction
345
THREAD INTERLEAVER 230
SELECTION UNIT 310
475
FF 455
Cntrl MUX 440
450
Sel MUX 320
Thread Conditions
245
265
High Priority Unit 420
Low Priority Unit 430
385
325
Instruction Queue 225

FIG. 4

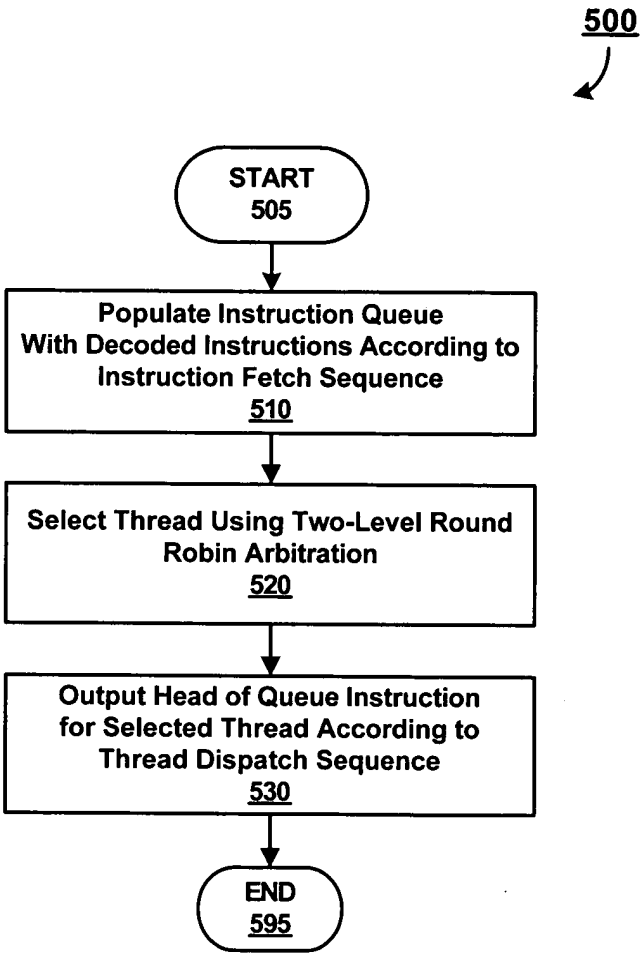
500
START
505
Populate Instruction Queue With Decoded Instructions According to Instruction Fetch Sequence
510
Select Thread Using Two-Level Round Robin Arbitration
520
Output Head of Queue Instruction for Selected Thread According to Thread Dispatch Sequence
530
END
595

FIG. 5A

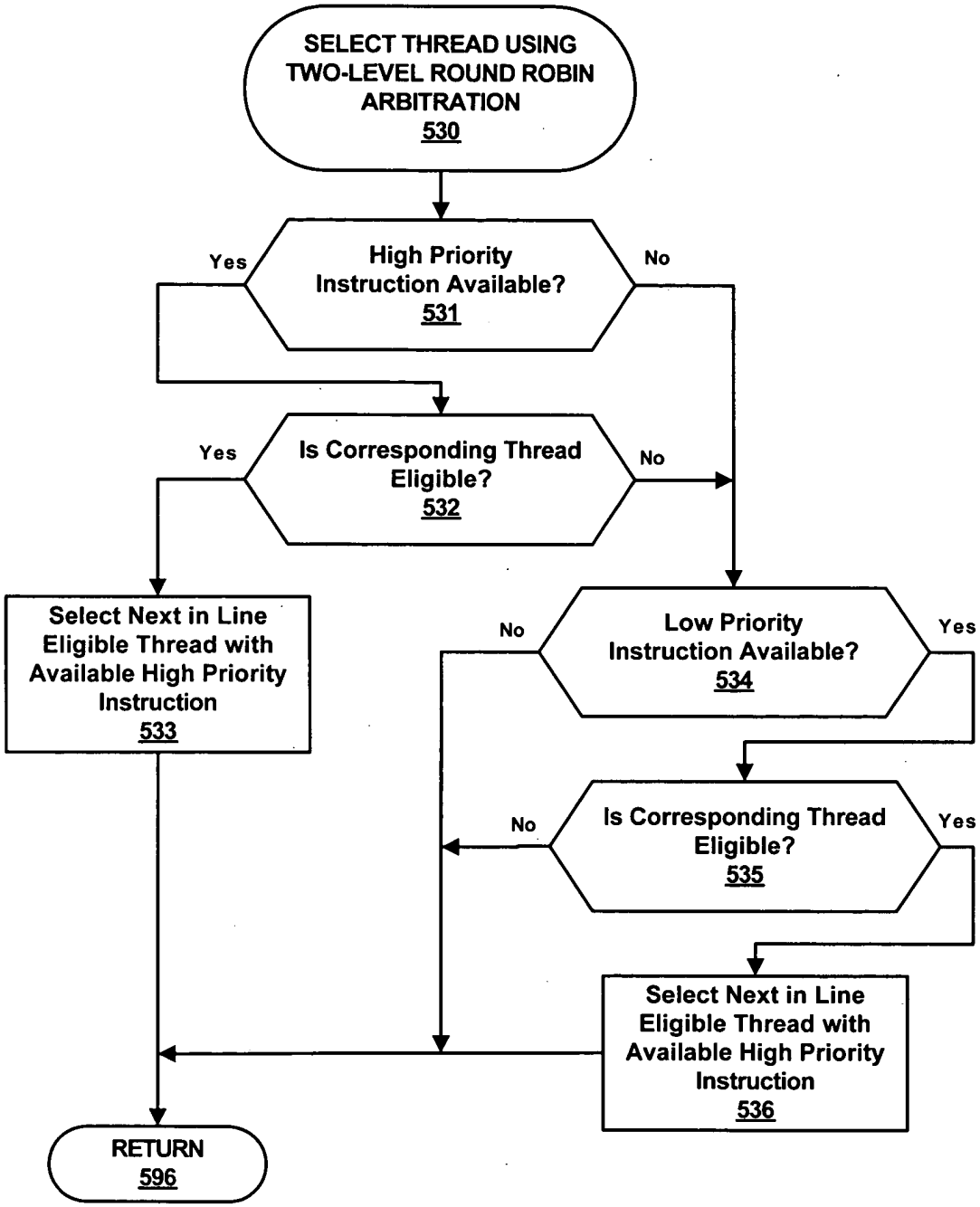
SELECT THREAD USING TWO-LEVEL ROUND ROBIN ARBITRATION
530
High Priority Instruction Available?
531
Yes
No
Is Corresponding Thread Eligible?
532
Yes
No
Select Next in Line Eligible Thread with Available High Priority Instruction
533
Low Priority Instruction Available?
534
No
Yes
Is Corresponding Thread Eligible?
535
No
Yes
Select Next in Line Eligible Thread with Available High Priority Instruction
536
RETURN
596

FIG. 5B

[Priority / Availibility / Eligibility]
610

	T_1	T_2	T_3	T_4	Previous Selection
t	[0/1/1]	[0/0/0]	[1/1/1]	[0/1/0]	—
t+1	[0/1/1]	[1/1/1]	[1/0/1]	[1/1/0]	T_3^1
t+2	[0/1/1]	[0/0/1]	[1/0/1]	[1/1/0]	T_2^1
t+3 (global stall)	[0/0/0]	[0/1/0]	[1/0/1]	[1/1/1]	T_1^1
t+4	[0/0/0]	[1/1/0]	[1/0/1]	[1/1/1]	—
t+5	[0/0/0]	[1/1/1]	[1/1/1]	[0/1/1]	T_4^1
t+6	[0/0/0]	[1/1/0]	[1/1/1]	[0/1/0]	T_2^2

Time

620

FIG. 6A

Express Mail Label No. EV 333134391 US
Title: Thread-Aware Instruction Fetching In A Multithreaded Embedded Processor
Inventors: Donald Steiss *et al.*
Atty. Docket No.: 22347-08564 (8422)
Sheet 7 of 13

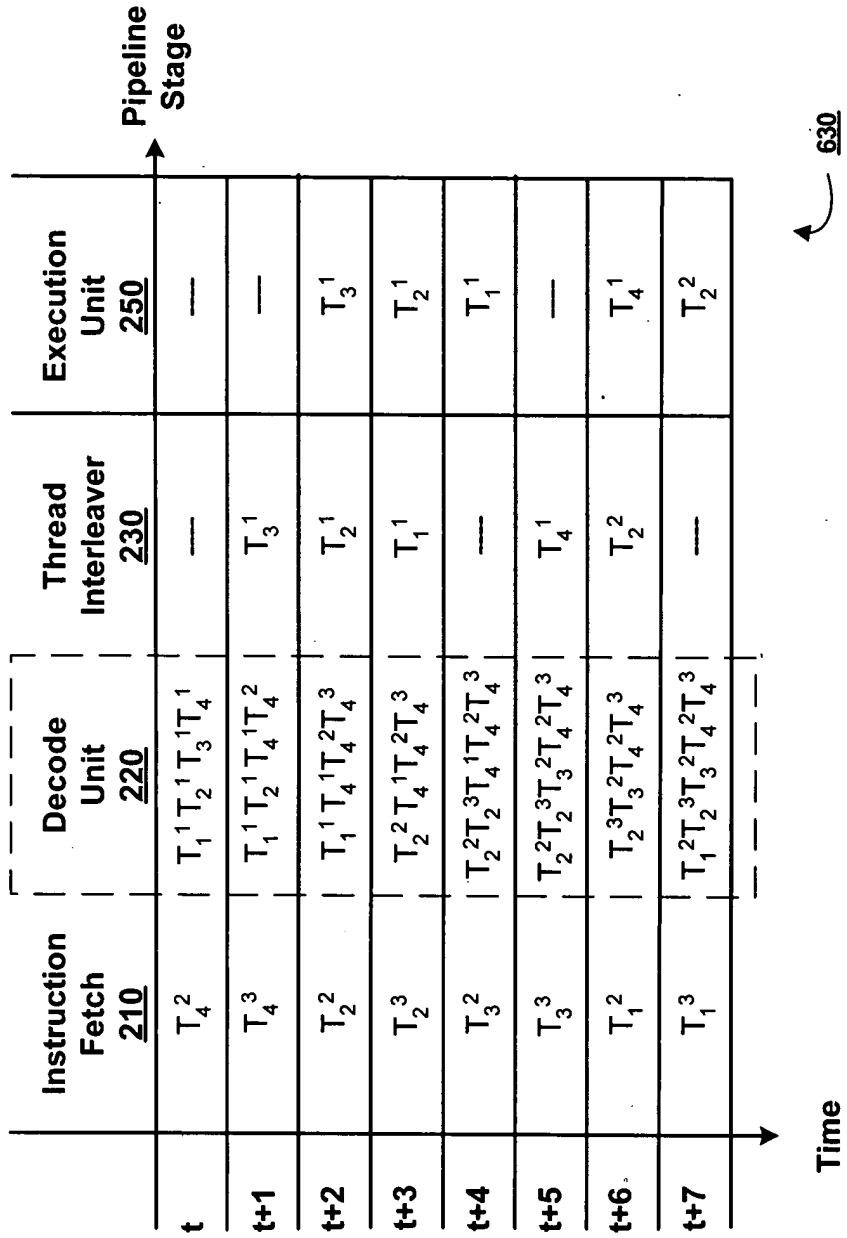
Pipeline Stage
Instruction Fetch 210
Decode Unit 220
Thread Interleaver 230
Execution Unit 250
630
Time
t
t+1
t+2
t+3
t+4
t+5
t+6
t+7

FIG. 6B

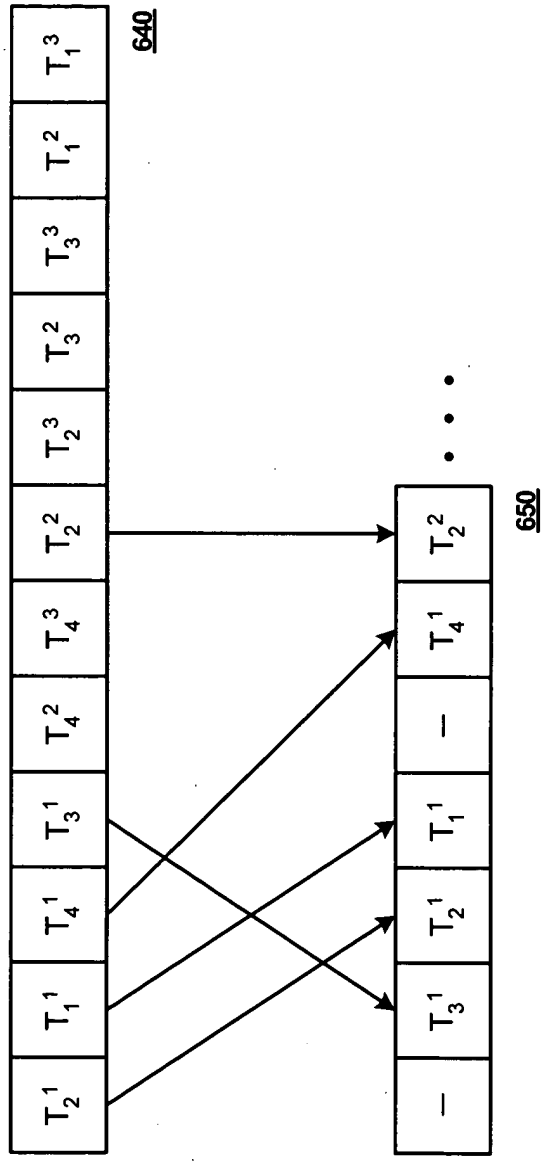
640
650
T_1^3
T_1^2
T_3^3
T_3^2
T_2^3
T_2^2
T_4^3
T_4^2
T_3^1
T_4^1
T_1^1
T_2^1
T_2^2
T_4^1
—
T_1^1
T_2^1
T_3^1
—

FIG. 6C

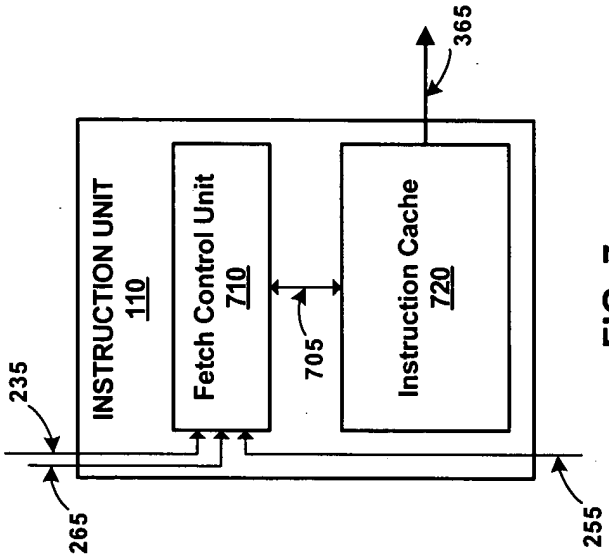
365
INSTRUCTION UNIT
110
Fetch Control Unit
710
705
Instruction Cache
720
235
265
255

FIG. 7

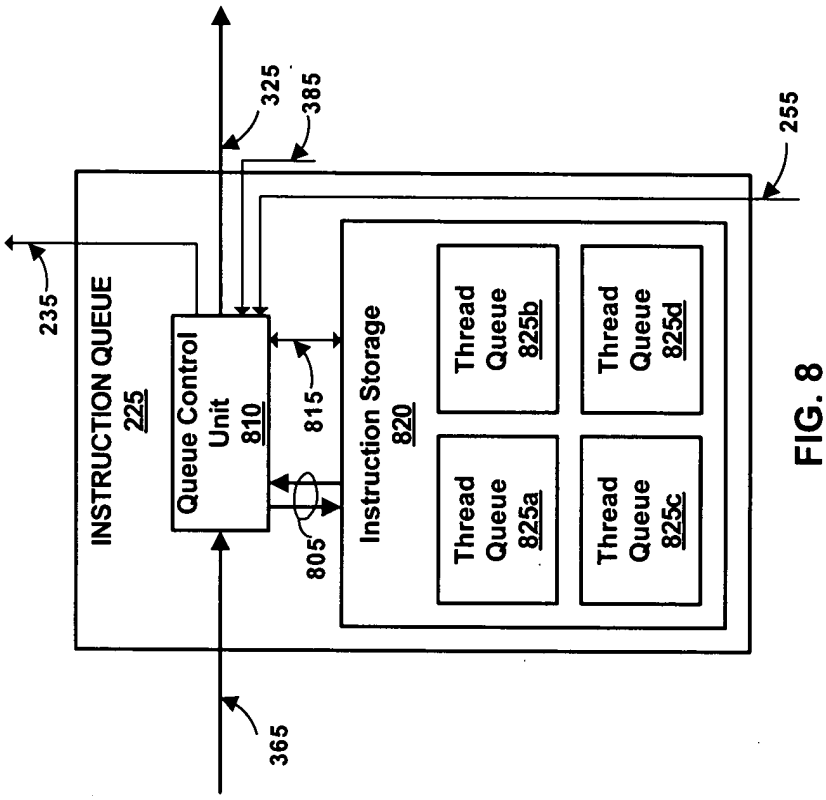
325
385
255
235
INSTRUCTION QUEUE
225
Queue Control Unit
810
815
805
Instruction Storage
820
Thread Queue
825b
Thread Queue
825d
Thread Queue
825a
Thread Queue
825c
365

FIG. 8

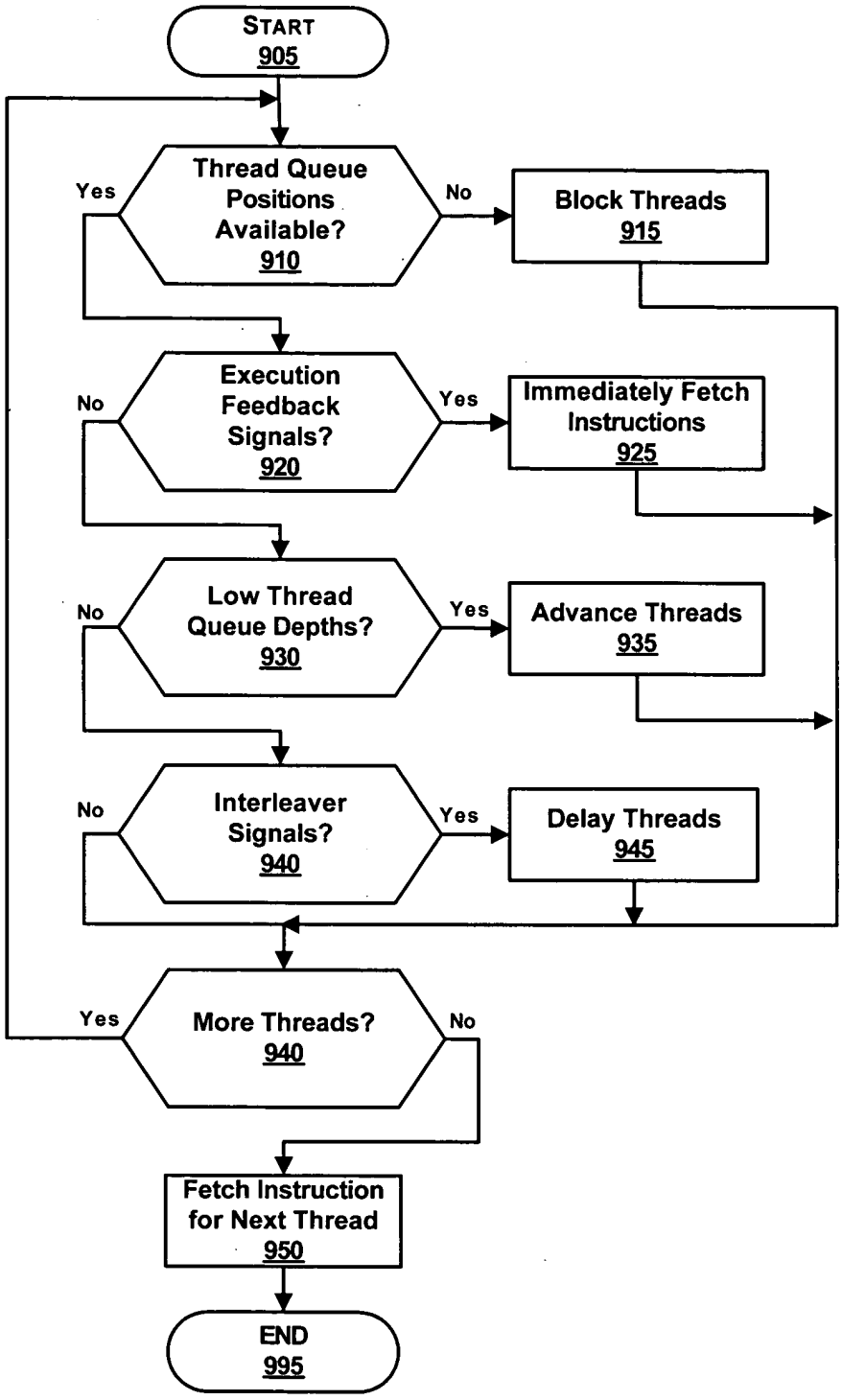
900
START
905
Thread Queue Positions Available?
910
Yes
No
Block Threads
915
Execution Feedback Signals?
920
No
Yes
Immediately Fetch Instructions
925
Low Thread Queue Depths?
930
No
Yes
Advance Threads
935
Interleaver Signals?
940
No
Yes
Delay Threads
945
More Threads?
940
Yes
No
Fetch Instruction for Next Thread
950
END
995

FIG. 9

[No Queue Position Available / Branch Misprediction / Low Queue Depth / Ineligible for Execution]

1010

	T_1	T_2	T_3	T_4	Fetch Control Unit 710
t	[0/0/0/0]	[0/0/0/0]	[0/0/0/0]	[0/1/0/0]	Immediately Fetch for T_4
t+1	[1/0/0/0]	[0/0/0/0]	[0/0/0/0]	[0/0/0/0]	Block Fetch for T_1
t+2	[0/0/0/0]	[0/0/1/0]	[0/0/0/0]	[0/0/0/0]	Advance Fetch for T_2
t+3	[0/0/0/0]	[0/0/0/0]	[0/0/0/0]	[0/0/0/0]	No Input for Response
t+4	[0/0/0/0]	[0/0/0/0]	[0/1/0/0]	[0/1/0/0]	Immediately Fetch for T_3

Time

1020

FIG. 10A

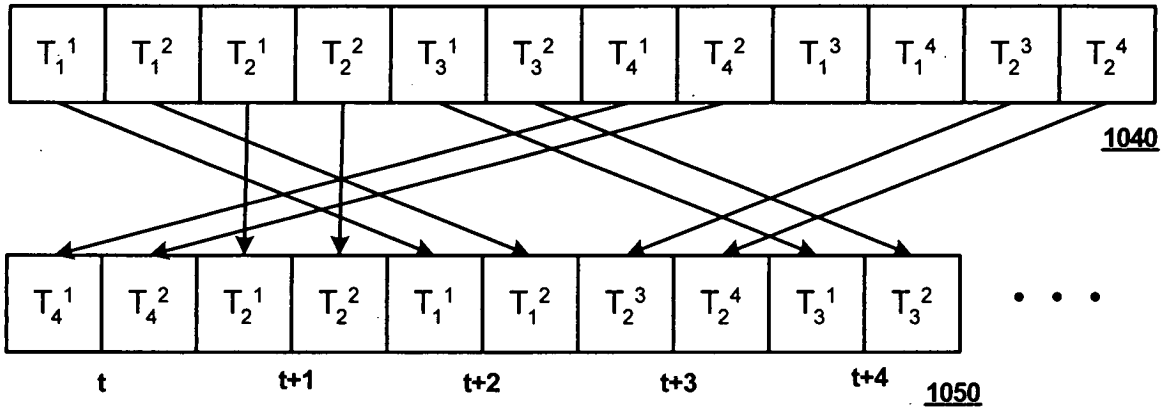

FIG. 10B

Express Mail Label No. EV 333134391 US
Title: Thread-Aware Instruction Fetching In A Multithreaded Embedded Processor
Inventors: Donald Steiss *et al.*
Atty. Docket No.: 22347-08564 (8422)
Sheet 13 of 13